**Amendments to the Specification:**

Please replace the paragraph from lines 13-22 on page 12 with the following amended paragraph:

-- An exemplary configuration of the input differential amplifier 1 is illustrated in Fig. 4. Accordingly, the differential amplifier 1 has two field-effect transistors T1, T2, to whose gate terminals the input clock signals Ap, An are applied. The source terminals are interconnected and connected to a current source S1. The drain terminals of the two transistors T1, T2 are respectively connected to a Vdd supply voltage via a resistor R7, R8. Furthermore, the ~~gate terminals~~ drain terminals of the transistors T1, T2 are connected to outputs at which the first and second amplified signals Bp, Bn are present. --

Please replace the paragraph from lines 8-20 on page 13 with the following amended paragraph:

-- Although the amplified output signal Bb, Bn of the first differential amplifier 1 eliminates disturbances of the type described in Figs. 1C to 1E, the differential amplifier 1 may also be defective. Moreover, there may be an offset on the line that the differential amplifier 1 cannot eliminate. Such an offset is illustrated in ~~Fig. 1D~~ Fig. 1B. Unlike in Fig. 1A, which shows an undistorted, ideal signal, a signal with a DC voltage (DC) offset is present in ~~Fig. 1D~~ Fig. 1B. Such a

DC voltage offset may occur in the case of so-called current mode level signals (CML) and is caused for example by unequal load resistances or switching transistors. The pulse widths T high and T_low are shifted on account of the offset. Furthermore, the signal-to-noise ratio decreases and the differential amplitude decreases, as can be discerned in the clock phase T_high. --

Please amend the paragraph from lines 15-24 on page 16 with the following amended paragraph:

-- A further circuit section of the generator circuit of Fig. 2 is realized by a controller for driving the two inverters In1, In2. The inverters In1, In2 are illustrated in Fig. 8. They are customary CMOS inverters with two MOS transistors T17, T18, a ~~p-channel~~ n-channel MOS transistor T17 and ~~an n-channel~~ a p-channel MOS transistor T18, which are of complementary configuration and are connected in series. The transistor T17 is connected to the reference-ground potential GROUND by its source terminal and the transistor T18 is connected to the operating voltage Vdd by its source terminal.

Please amend the paragraph from line 20 on page 18 to line 4 on page 19 with the following amended paragraph:

-- The second input signal for the integrator is likewise provided by a voltage divider 5 with the resistors R3, R4 and

a capacitor C2. The voltage divider 5 provides a desired value. The difference between the input signals is integrated by the ~~integrator 7~~ integrator 8. The ~~integrator 7~~ integrator 8 then makes a control voltage Vcmc available to the third differential amplifier 3, which is connected downstream of the second differential amplifier 2 and outputs the drive signals for the two inverters In1, In2. --

Please amend the paragraph from line 12 on page 19 to line 7 on page 20 with the following amended paragraph:

-- The third differential amplifier 3 is illustrated in Fig. 5A. The output voltage Vcmc of the second integrator serves for controlling a current source S6 of the third differential amplifier. The latter, in a manner similar to the differential amplifiers described above, furthermore has two input transistors T15, T16, a current source S7 and two resistors R9, R10, R11, a respective one of the resistors R9, R10 being connected between the drain terminal of the transistors T15, T16 and the ~~voltage Vdd~~ resistor 11. The control voltage Vcmc provided by the integrator 8 is then used to provide a current Icmc that flows to the current source S6 via a resistor R11. By using the current Icmc and the resistor R11, an offset voltage is superposed on the signal voltages Dp, Dn at the outputs of the third differential amplifier 3. As a result, the input pulse shape in accordance

with Fig. 9 can be shifted to the optimum switching point of the inverter and an optimum output pulse shape can be achieved. In this case, on account of the previous circuit measures, it is assumed that the differential signal Dp, Dn has already been set optimally and only the level position, i.e. the offset for the inverter switching point, is to be set. --

**Amendments to the Drawings:**

The attached sheet of drawings includes changes to Fig. 9. This sheet, which includes Fig. 8 replaces the original sheet including Figs. 8 and 9. Specifically, the parameter $U_{out}$ has been changed to $U_{in}$.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes